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UNITED STATES PATENT APPLICATION

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for

LEVEL SHIFTER WITHOUT DUTYCYCLE DISTORTION

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LEVEL SHIFTER WITHOUT DUTYCYCLE DISTORTION

[0001] This application claims priority of pending German Patent Application No. 102 30 168.9 filed on July 4, 2002.

Field Of The Invention

[0002] The invention involves a voltage converter in terms of the main concept of Claim 1.

[0003] With semi-conductor components, especially memory modules such as DRAMs (DRAM = Dynamic Random Access Memory or dynamic read/write memories) the voltage level used inside a component may differ from the voltage level used on the outside.

[0004] In particular, the internally used voltage level may be lower than the externally used voltage level; for instance, the internally used voltage level may amount to 1.8 V and the externally used voltage level to 2.5 V.

[0005] This may be due to the fact that the externally supplied voltage may for instance be subject to relatively large fluctuations and therefore usually needs to be converted to a particular internal voltage (regulated to a constant value and subject to relatively minor fluctuations only) by means of a voltage regulator, to permit the component to operate in a fault-free fashion.

[0006] The use of a voltage regulator will necessarily cause a voltage drop, which means that the internal voltage level used inside the component will be lower than the external voltage.

[0007] An internal voltage lower than the external voltage has the advantage of being able to reduce power dissipation in semi-conductor components.

[0008] Where a lower internal than external voltage is used in components, the signals generated inside the components must first be converted into signals at a correspondingly higher voltage by means of a so-called voltage converter before being emitted.

[0009] Such voltage converters may for instance contain an amplifier circuit consisting of cross-connected p or n channel field effect transistors.

[00010] The lower voltage signals internally generated in a component may be changed into correspondingly higher voltage signals – retarded with a certain delay - by means of such an amplifier circuit.

[00011] In the process, the delay occurring at the positive flank of an internal signal may differ from the delay occurring at the negative flank of the internal signal. This causes the higher-voltage signals emitted by the amplifier circuit to be distorted.

[00012] To counter this effect, the signals emitted by the amplifier circuit may be conducted to a driver stage with several - for instance two - series-connected inverters.

[00013] The inverters are arranged in such a way that the distortions contained in the signals emitted by the amplifier circuit are compensated.

[00014] The driver stage will in any event cause a relatively high – additional – signal delay; furthermore the above signal distortions can only be partially compensated by means of a voltage converter of the above kind, due

to changes to the characteristics of the voltage converter components caused by temperature fluctuations.

[00015] This invention is designed to provide a novel voltage converter mechanism.

[00016] This and other aims are achieved by the subject matter as defined by Claim 1.

[00017] Further beneficial aspects are contained in the subclaims.

[00018] In terms of a basic concept of the invention, a voltage converter device is provided to convert a signal at an initial voltage level (vint) into a signal at a secondary voltage level that differs from the first voltage level (vint), for which purpose the voltage converter mechanism has an amplifier device, and whereby for the generation of the signal at the secondary voltage level (vddq) a second amplifier device output signal, different to a first amplifier device output signal – in particular complementary to it -, is used.

[00019] Advantageously, one flank of the first amplifier output signal triggers the signal at the secondary voltage level (vddq) so that it changes from a first to a second state, and a flank of the second amplifier output signal, displaced in time in relation to the flank of the first amplifier output signal, triggers the signal at the secondary voltage level (vddq) so that it changes from the second back to the first state.

[00020] It is preferable that the triggering flank of the first amplifier output signal is a positive flank, and the triggering flank of the secondary amplifier output signal is a positive flank as well (or alternatively the triggering

flanks of the first and second amplifier output signals both are negative flanks).

[00021] With such a voltage converter device it may for instance be possible to almost completely compensate the distortions contained in the amplifier circuit output signals, even at relatively high temperature fluctuations.

Brief Description of the Drawings

[00022] Below, the invention is more clearly illustrated by means of an embodiment and the attached drawings. The drawings show the following:

[00023] Figure 1 a schematic representation of the switching device of a current state-of-the-art voltage converter;

[00024] Figure 2a a schematic representation of the first section of the switching device of a voltage converter as it appears in an embodiment of the above invention;

[00025] Figure 2b a schematic representation of another section of the switching device of the voltage converter as it appears in an embodiment of the above invention; and

[00026] Figure 3 a schematic representation of the chronological progress of the input and output signals of the amplifier circuit in the voltage converter illustrated in Figures 2a and 2b, and the distortion-free output signal of the voltage converter.

Detailed Description of the Drawings

[00027] Figure 1 shows a schematic representation of a switching device of a state-of-the-art voltage converter 1. The voltage converter 1 has been installed into a DRAM memory component; for instance one based on CMOS technology. It is used to convert a voltage level used inside the memory modules (vint) to a voltage level used outside the memory modules (vddq), where the internally used voltage level (vint) is lower than the externally used voltage level (vddq). The internal voltage (vint) may for instance amount to 1.8 V, and the external voltage level (vddq) to 2.5 V.

[00028] As shown in Figure 1, the voltage converter 1 has an amplifier circuit 2, and a driver stage 8 with a first and a second inverter 3a, 3b (as well as further alternative inverters not shown here).

[00029] The amplifier circuit 2 consists of four cross-connected transistors, i.e. a first and a second p-channel field effect transistor 4a, 4b (here two p-channel MOSFETs 4a, 4b), as well as a first and a second n-channel field effect transistor 5a, 5b (here two n-channel MOSFETs 5a, 5b).

[00030] The source of the first n-channel field effect transistor 5a is earthed to ground (gnd). In the same way the source of the second n-channel field effect transistor is earthed to ground (gnd).

[00031] In addition, the gate of the first n-channel- field effect transistor 5a is connected to a first input 6a of the amplifier circuit 2, and the gate of the second n-channel field effect transistor 5b to a second amplifier circuit input 6b.

[00032] The drain of the first n-channel field effect transistor 5a is connected to a first output 7a, as are the gate of the second p-channel field

effect transistor 4b, and the drain of the first p-channel field effect transistor 4a. In the same way a second amplifier circuit output 7b is connected to the drain of the second n-channel field effect transistor 5b, as well as to the gate of the first p-channel field effect transistor 4a, and to the drain of the second p-channel field effect transistor 4b.

[00033] The source of the first and second p-channel field effect transistors 4a, 4b is also connected to the supply voltage. This carries – as described above – a relatively high voltage level (vddq) compared to the internally used voltage.

[00034] A first internal signal (in) is carried to the first input 6a of the DRAM memory components, and a second component-internal signal (bin) to the second input 6b of the amplifier circuit 2.

[00035] The first and second internal signals (in or bin) are complementary to each other.

[00036] The "high logic" states of the first or second internal signals (in or bin) are essentially of equal duration to their "low logic" states. The internal signals (in or bin) carry – as illustrated above – the relatively low internally used voltage (vint) in comparison to the (higher) externally used voltage level (vddq).

[00037] With the help of the amplifier circuit 2 the internal signal (in) at the first input 6a of the amplifier circuit 2 is converted into a signal (out) corresponding to this signal (in) and accessible at the second output 7b of the amplifier circuit. This signal (out) carries the above-mentioned relatively high external voltage level (vddq).

[00038] If the internal signal present at the first input 6a of the amplifier circuit changes from a "high logic" to a "low logic" state (and the complementary internal signal (bin) from a "high logic" state to a "low logic" state), the corresponding signal (out), accessible at output 7b of the amplifier circuit 2 only changes from the "low logic" to the "high logic" state after a particular delay period dl' as a result of internal signal delay times in the amplifier circuit 2.

[00039] In the same way, a change in the state of the internal signal (in) from "high logic" to "low logic" (and a change of the state of the complementary internal signal (bin) from "high logic "to "low logic") causes the corresponding signal (out) to change from the "high logic" to the "low logic" state after a particular delay period d2'.

[00040] The delay period dl' inside amplifier circuit 2 – occurring at a positive flank of the internal signal (in) – differs from the internal delay period d2' in the amplifier circuit 2 at a negative flank of the internal signal (in) as a result of differing signal delay times in the amplifier circuit 2. This causes distortion of the signal (out) accessible at 7b (especially because its "high logic" state lasts longer than its "low logic" state, and is not essentially of the same duration, which would be ideal.)

[00041] To counteract this effect, the signal (out) accessible at output 7b of the amplifier circuit 2 is connected by means of a conductor 9 to an input of the first inverter 3a, whose output 11 is connected to an input of the second inverter 3b by means of a conductor 10.

[00042] During a change in the state of the signals (out) accessible at output 7b of the amplifier circuit from "low logic" to "high logic" (or conversely when the state of the signals "out" change from "high logic" to "low logic") the signal at output 11 of the first inverter 3a changes its state from "high logic" to

"low logic"(or conversely, from "low logic" to "high logic"), according to delay times that differ from each other; consequently he output signal (DatoV) accessible at an output 12 of the second inverter 2b, also changes from a "low logic" state to a "high logic" state, or conversely from a "high logic" to a "low logic" state (again according to delay times that differ from each other).

[00043] The inverters 3a, 3b – especially the varying delay times caused by them, which differ from positive to negative signal flanks – are so arranged that the delay time dl occurring between the signal (in) present at the positive signal flank of input 6a of the amplifier 2, and the corresponding output signal (DatoV) emitted by the positive signal flank at the second inverter 3b, is as large in total as the delay time d2 occurring between the negative signal flank of the signal (in) and a corresponding negative signal flank of the output signal (DatoV).

[00044] In this way compensation of the distortion of the signal (out) present at output 7b of the amplifier circuit is maintained (so that, for instance, a "low logic" state of the output signal (DatoV) at output 12 of the second inverter 3b essentially lasts as long as its "high logic" state).

[00045] The driver stage 8 leads to a relatively high (additional) signal delay; furthermore, due to component inaccuracies or changes in the characteristics of components caused by temperature fluctuations, the distortions caused by a voltage converter of the type described above can only be partially compensated.

[00046] Figure 2a is a schematic representation of the first section 101a of a circuit configuration of a voltage converter according to an embodiment of the present invention.

[00047] The voltage converter is installed in a CMOS technology based memory component and is especially suited to be used as an OCD (off-chip driver) component of the DRAM memory components, or for instance as a DLL (delay locked loop) component.

[00048] By means of the voltage converter an internal voltage level (vint) used inside the DRAM memory components is changed into an external voltage level (vddq) used outside the memory components – here the internally used voltage level (vint) is lower than the externally used voltage level (vddq).

[00049] The internal voltage level (vint) may for instance amount to 1.8 V - or alternatively 1.5 V, and the external voltage level (vddq) for example to 2.5 V or also to 1.8 V, for example.

[00050] Figure 2a shows that the first section 101a of the voltage converter contains an amplifier circuit 102, and two parallel driver stages, each containing an inverter 103a, 103b as well as a transmission gate or transfer element 113a, 113b.

[00051] The amplifier circuit 102 consists of several transistors, in particular four cross-connected ones: a first and a second p-channel field effect transistor 104a, 104b (here two p-channel MOSFETs 104a, 104b), as well as a first and a second n-channel field effect transistor 105a, 105b (here two n-channel MOSFETs 105a, 105b).

[00052] The source of the first n-channel field effect transistor 105a is earthed to ground (gnd). In the same way the source of the second n-channel field effect transistor 105b is also earthed to ground (gnd).

[00053] Furthermore the gate of the first n-channel field effect transistor 105a is connected to a first input 106a of the amplifier circuit 102, and the gate of the second n-channel field effect transistor 105b to a second amplifier circuit input 106b.

[00054] The drain of the first n-channel field effect transistor 105a is connected to a first input 107a of the amplifier circuit 102, as well as to the gate of the second p-channel field effect transistor 104b, and to the drain of the first p-channel field effect transistor 104a. In the same way a second amplifier circuit output 107b is connected to the second n-channel field effect transistor 105b, as well as to the gate of the first p-channel field effect transistor 104a, and to the drain of the second p-channel field effect transistor 104b.

[00055] The sources of the first and second p-channel field effect transistors 104a, 104b are both connected to the supply voltage. As mentioned above, this supply is at a relatively high voltage level (vddq) compared to the internally used voltage.

[00056] The amplifier circuit 102 carries a first internal signal (in) of the DRAM memory components to the first input 106a, and a second component–internal signal (bin) to the second input 106b of the amplifier circuit 102.

[00057] The first and second internal signals (in or bin) are complementary to each other.

[00058] In addition, the "high logic" states of the first or second internal signals (in or bin) last as long as their "low logic" states.

[00059] As mentioned above, the internal signals (in or bin) carry the relatively lower internally used voltage level (vint), compared to the externally used voltage level (vddq).

[00060] With the help of the amplifier circuit 102 the internal signal (in) at the first amplifier circuit input 106a is changed into a corresponding signal (out) accessible at the second output 107b of the amplifier circuit 102, as well as into a signal (bout) complementary to this signal (out), which can be tapped at the first output 107a of the amplifier circuit 102.

[00061] The signals (out or bout), accessible at the first and second amplifier circuit outputs 107a, 107b carry the relatively high external voltage level (vddq), compared to the voltage level (vint) used in internal signals.

[00062] If the internal signal (in) present at the first input 106a of the amplifier circuit 102 changes from a "low logic" to a "high logic" state (and the complementary internal signal (bin) from a "high logic" to a "low logic") state, then according to Figure 3, the signal (out) present at the second output 107b of the amplifier circuit 102 only changes its state from "low logic" to "high logic", after a certain delay period d1' due to internal signal delays inside the amplifier circuit (and – after a delay period d2"that differs from the delay period d1' - the signal (bout) present at the first output 107a changes from "high logic" to "low logic").

[00063] Similarly, during a change in the states of the internal signal (in) from "high logic" to "low logic" (and a change in the state of the complementary internal signals (bin) from "low logic" to "high logic") then according to Figure 3 the signal (out) present at the second output 107b only changes its state from "high logic " to "low logic" after a certain delay period d2' (and – after a delay period d1"that differs from the delay period d2' – the

signal (bout) present at the first output 107a changes from "low logic" "high logic").

[00064] Due to varying internal delay periods inside the amplifier circuit, the delay period d1' occurring at a positive flank of the internal signal (in) on the signal (out), (or at negative flank of the complementary signal (bin)), differs from the delay period d2' occurring at a negative flank of the internal signal (in) on the signal (out), (or at a positive flank of the complementary signal (bin)).

[00065] Similarly the delay period d2" occurring at a positive flank of the internal signal (in) at the complementary signal (bout), differs from the delay period d1"occurring at a negative flank of the internal signal (in) on the complementary signal (bout).

[00066] This has the effect – as shown in Figure 3 – that the signals (out or bout) present at the first and second outputs 7a, 7b are distorted (especially that their "low logic" states last longer than their "high logic" states and not, which would be ideal, that they last equally long.)

[00067] The compensate this effect, a characteristic of the voltage converter shown in Figures 2a and 2b is used (also shown in Figure 3) namely that the delay period d1' occurring at a positive flank of the internal signals (in) on the signal (out) is as long – due to the symmetrical construction of the amplifier circuit 102 – as the delay period d1" occurring at a negative flank of the internal signals (in) on the complementary signal (bout) (or conversely, that the delay period d2' occurring at a negative flank of the internal signal (in) on the signal (out) is as long as the delay period d2"occurring at a positive flank of the internal signal (in) on the complementary signal (bout)).

[00068] As shown in detail in Figure 2a, the signal (out) present at the second output 107b of the amplifier circuit 102 of the voltage converter is connected by means of a conductor 109b to an input of the second inverter 103b according to the prototype shown, while the complementary signal (bout) present at the first output 107a of the amplifier circuit 102 is connected to an input of the first Inverter 103a.by means of a conductor 109a.

[00069] Both inverters 103a, 103b consist of an n- and a p-channel field effect transistor each, while the source of each n-channel field effect transistor is earthed to ground (gnd), and the source of each p-channel field effect transistor to the supply voltage (vddq). The field effect transistors used in the inverters 103a, 103b are thus always working in the source circuit, and amplify input voltages present at each inverter input by inversion, whereby each of the field effect transistors of the inverters 103a, 103b constitute the operating resistance for every other field effect transistor.

[00070] As shown in Figures 2a and 2b, the signal (out), present at the second output 107b of the amplifier circuit 102, has an additional connection (apart from conductor 109b connected to the second inverter 103b) to the first control input of the transmission gate 113b by means of a conductor 111b.

[00071] Similarly the complementary signal (bout) present at the first output 107a of the amplifier circuit 102 has an additional connection (apart from the connection to the first Inverter 103a by means of conductor 109a) to the first control input of the first transmission gate 113a by means of the conductor 111a.

[00072] As further shown in Figures 2a and 2b, the output of the first Inverter 103a is connected by means of conductor 110a to a second, complementary control input of the first transmission gates 113a, and the

output of the second inverter 103b to a second, complementary control input of the second transmission gate 113b by means of a conductor 110b.

[00073] The transmission gates 113a, 113b have an n-, and a p-channel field effect transistor each, while each first control input of transmission gates 113a, 113b is connected to the gate of the first, and each second, complementary control input of transmission gates 113a, 113b is connected to the gate of the second field effect transistor.

[00074] In addition the drain or source of the n- or p-channel field effect transistor of the first transmission gate (i.e. the inlet or output of the first transmission gate 113a) is connected to ground (gnd), or to an output 112 of the voltage converter by means of a conductor 114a.

[00075] In contrast, the source of the n- or p-channel field effect transistor (i.e. the inlet or output of the second transmission gate 113b) is connected to the supply voltage (vddg), or by means of conductor 114b to the voltage converter output 112.

[00076] This has the following effect: as soon as the signal (out) tapped at the second output 107b of the amplifier circuit 102 and connected to the first control input of the second transmission gate 113b by means of the conductor 111b, changes from "low logic" to "high logic" (and the complementary signal (outb) fed in via the conductor 110b changes from "high logic" to "low logic"), the supply voltage (vddq) at the input of the second transmission gate 113b is switched through to the transmission gate output, and from there via conductor 114b to the voltage converter output 112.

[00077] In this way, as illustrated in Figure 3, the output signal present at the voltage converter output 112 (DatoV) changes from a "low logic" to a "high logic" state.

[00078] If the signal (out), tapped at the second output 107b of the amplifier circuit 102 then again changes from "high logic" to "low logic"(and the complementary signal (outb) changes from "low logic" to "high logic"), the supply voltage (vddq) present at the input of the second transmission gate 113b is again disconnected from the second transmission gate 113b; the output signal (DatoV) at voltage converter output 112 as shown in Figure however still stays at the "high logic" state.

[00079] Only then, when the signal (bout), tapped at the first output 107a of the amplifier circuit 102 and connected via conductor 111a to the first control input of the first transmission gate 113a, changes from "low logic" to "high logic" (and the complementary signal (boutb) from "high logic" to "low logic"), does the first transmission gate 113a and consequently the output of the first transmission gate 113a become conductive - and via conductor 114a also the output 112 of the voltage converter – and earthed to ground (gnd).

[00080] In the process, as illustrated in Figure 3, the output signal (DatoV) present at the voltage converter output 112 changes from a "high logic" to a "low logic" state.

[00081] If the signal (bout) tapped at the first output 107a of the amplifier circuit 102 then again changes its state from "high logic" to "low logic", the input of the first transmission gate 113a is again disconnected from its output; the output signal (DatoV) at the voltage converter output 112 however still remains at a "low logic" state as shown in Figure 3 (because the inlet and output at the second transmission gate 113a are disconnected from each other for the time being, i.e. the supply voltage (vddq) present at the input of the second transmission gate 113b has not yet been connected to its output).

[00082] The output signal (DatoV) present at the voltage converter output 112 then – in contrast to the signals (bout or out) present at outputs 107a or 107 of the amplifier circuit 102 - shows no (or only negligible) distortion; in particular the "low logic" state of the output signal (DatoV) is essentially equal in length to its "high logic" state.

[00083] The voltage converter shown in Figures 2a and 2b only experiences relatively minor (additional) signal distortion. In addition, the distortions in the amplifier circuit output signals (bout or out) are almost completely compensated by the voltage converter as shown in Figures 2a and 2b, even at high temperature fluctuations (and the consequent changes in the characteristics of components used).

Reference list

1	Voltage converter
2	Amplifier circuit
3a	Inverter
3b	Inverter
4a	p-Channel field effect transistor
4b	p-Channel field effect transistor
5a	n-Channel field effect transistor
5b	n-Channel field effect transistor
6a	Input
6b	Input
7a	Output
7b	Output
8	Driver stage
9	Conductor
10	Conductor
11	Output
12	Output
101a	Voltage converter section
101b	Voltage converter section
102	Amplifier circuit
103a	Inverter
103b	Inverter
104a	p-Channel field effect transistor
104b	p-Channel field effect transistor
105a	n-Channel field effect transistor
105b	n-Channel field effect transistor
106a	Input
106b	Input
107a	Output
107b	Output
109a	Conductor
109b	Conductor
110a	Conductor
110b	Conductor
111a	Conductor
111b	Conductor
112	Output
113a	Transmission gate
113b	Transmission gate
114a	Conductor
114b	Conductor